

IN THE CLAIMS:

1. (Original) A semiconductor device including an MIM capacitor, the semiconductor device comprising:
 - a semiconductor substrate;
 - an interlevel dielectric film provided on the semiconductor substrate; and
 - an interconnect buried in the interlevel dielectric film and electrically connected to the semiconductor substrate,wherein the MIM capacitor includes a first electrode of a metal, a second electrode of a metal and a capacitive insulating film of a dielectric,
 - the first electrode is buried in the interlevel dielectric film,
 - the capacitive insulating film is provided on the first electrode, and
 - the second electrode is a metal layer provided to face the first electrode with the capacitive insulating film interposed therebetween.
2. (Original) The semiconductor device of claim 1, wherein a pad electrode is provided and exposed on part of the interconnect, and
 - the pad electrode and the second electrode are made of the metal layer.
3. (Original) The semiconductor device of claim 1, wherein a pad electrode is provided and exposed on part of the interconnect,
 - a connecting line for electrically connecting another part of the interconnect to the second electrode is provided on the second electrode, and
 - the pad electrode and the connecting line are made of an identical metal film.

4. (Original) The semiconductor device of claim 1, wherein the capacitive insulating film is a film having a function of preventing diffusion of the metal constituting at least one of the first and second electrodes.

5. (Original) The semiconductor device of claim 1, wherein the capacitive insulating film is a film made of silicon nitride.

6-10. (Canceled)

11. (New) A semiconductor device comprising:
a substrate;
a first insulating film formed on the substrate;
at least two lower wires and a lower electrode formed in the first insulating film;
a second insulating film formed on the first insulating film,
a first upper wire and a second upper wire formed in the second insulating film,
and
a capacitive insulating film formed between the lower electrode and a first part of the first upper wire,
wherein the second upper wire, and a second part of the first upper wire are connected to the lower wires for each, and the second upper wire is electrically connected to a pad.

12. (New) The semiconductor device of claim 11, wherein a third insulating film is formed between the first insulating film and the second insulating film, the capacitive insulating film is a part of the third insulating film, both the second upper wire, and the second part of the first upper wire are connected to each of the lower wires through the third insulating film.
13. (New) The semiconductor device of claim 11, wherein the capacitive insulating film includes at least one selected from SiN, SiON, SiC, or SiOC.
14. (New) The semiconductor device of claim 11, wherein the pad is contacted with the second upper wire in the second insulating film.
15. (New) The semiconductor device of claim 11, wherein the lower electrode is placed at a distance from each of the lower wires.
16. (New) The semiconductor device of claim 11, wherein the lower wires and the lower electrode are made of an identical material.
17. (New) The semiconductor device of claim 11, wherein the first upper wire and the second upper wire are made of an identical material.
18. (New) The semiconductor device of claim 11, wherein a top surface of the first upper wire is covered by the second insulating film.

19. (New) The semiconductor device of claim 11, wherein the lower electrode or the upper electrode includes at least one selected from Cu, Al, Cu alloy, or Al alloy.

20. (New) A semiconductor device comprising:
a substrate;
a first insulating film formed on the substrate;
at least two lower wires and a lower electrode formed in the first insulating film;
an upper electrode, a first upper wire and a second upper wire formed on the first insulating film, and
a capacitive insulating film formed between the lower electrode and the upper electrode,
wherein a first part of the first upper wire is electrically connected with a top surface of the upper electrode, and a second part of the first upper wire is electrically connected with the lower wires,
the second upper wire is electrically connected to a pad and the lower wires.

21. (New) The semiconductor device of claim 20, wherein a top surface of the first upper wire is covered by a second insulating film.

22. (New) The semiconductor device of claim 21, wherein the first upper wire is placed at a distance from the second upper wire by the second insulating film.

23. (New) The semiconductor device of claim 20, wherein the capacitive insulating film is a part of a third insulating film,

both the second upper wire, and the second part of the first upper wire are connected to each of the lower wires through the third insulating film.

24. (New) The semiconductor device of claim 20, wherein the capacitive insulating film includes at least one selected from SiN, SiON, SiC, or SiOC.

25. (New) The semiconductor device of claim 20, wherein the lower wires and the lower electrode are made of an identical material.

26. (New) The semiconductor device of claim 20, wherein the first upper wire and the second upper wire are made of an identical material.

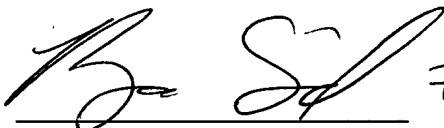
27. (New) The semiconductor device of claim 11, wherein the lower electrode or the upper electrode includes at least one of selected from Cu, Al, Cu alloy, or Al alloy.

Applicants believe that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicants have inadvertently overlooked the need for a petition for extension of time. The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0417. A duplicate copy of this Response is enclosed for accounting purposes.

Respectfully submitted,

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